WIDEBAND COMMUNICATION USING DELAY LINE CLOCK MULTIPLIER

ABSTRACT OF THE DISCLOSURE

A delay line clock multiplier is disclosed for use in a communication system, in which a delay line is used as a clock multiplier for generating a higher speed clock that may be used, for example, for data sampling. The speed and timing characteristics of the clock delay line are adjusted by controlling the supply voltage to the delay line. because proper synchronization may be achieved at the higher frequencies using an oversampling synchronization approach which in turn is made possible by the delay line clock multiplier which allows for the oversampling of a signal at sub-interval increments.